Thermal Cycling Test Results of CSP and RF Package Assemblies

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ABSTRACT

A JPL-led chip scale package (CSP) Consortium of enterprises, composed of representing government agencies and private companies, recently joined together to pool in-kind resources for developing the quality and reliability of chip scale packages (CSPs) for a variety of projects. Consortium assembled fifteen different packages from 48 to 784 I/Os and pitches from 0.5 to 1.27 mm on multilayer FR-4 printed wiring board (PWB). In addition, two other test vehicles built by two team members, each had a control wafer level CSP package for data comparison. Assemblies were subjected to numerous thermal cycling conditions including -55°C to 125°C. Cycles-to-failure (CTF) test results to 500 cycles for the control CSP assembly are presented. Also, CTF results of two fine pitch BGAs with 0.8 mm pitch and different die sizes for a test vehicle are compared. In addition, one of the test vehicle included a fine pitch BGA interconnect structure at Radio Frequencies (RF) using a 50-Ohm transmission line and resonant circuit. Return and insertion losses were determined prior to and after 500 cycles and presented.

INTRODUCTION

Chip Scale Packages (CSP) now widely used for many electronic applications including portable and telecommunication products. CSP definition has evolved as the technology matured and now are those packages with pitch of 0.8 mm and lower. Packages with fine pitches especially those with less than 0.8 mm may require the use of microvia printed wiring board (PWB) which is costly and they may perform poorly when are assembled on board. A test vehicle (TV1) with eleven different package types and pitches were build and tested by the JPL MicrotypeBGA Consortium during 1997 to 1999 and lessons learned by team were published as a guidelines document [1].

The finer pitch CSP packages which recently become available were included in the next test vehicle of the JPL CSP Consortium. Consortium team jointly concentrated their efforts on build of the second test vehicle (TV-2) with fifteen (15) packages from low to high I/O (48 to 784) and pitches of 0.5 mm to 1.27 mm. In addition to TV-2 test vehicle, other test vehicles designed and built by individual team members to meet their needs. At least one common package as control was included in these test vehicles in order to be able to compare the environmental test results and understand the effect of PWB build and manufacturing variables. One test vehicle was designed by Litton Corporation (Facility A) and were built at two manufacturing sites, herein refer to TV-L. The other test vehicle was designed and assembled by Hughes Network System (Facility B) using their internal resources and is identified as TV-H. Also, TRW (Facility C) designed and built two RF packages with 0.75 mm fine pitch BGA interconnects and assembled on the TV-L. In this paper preliminary thermal cycling test results performed under -55 to 125°C to 500 thermal cycles are presented. RF characteristic of interconnects prior to and after 500 cycles also are presented. Correlation of print paste quality and volume for the TV-2 is discussed in another paper published in this proceeding[2].

CSP TEST MATRIX

Aspects of the three test vehicles build are discussed below. These are:

- TV-2, the 2nd test vehicle which was designed and built by the CSP Consortium team members.
- TV-L, designed by Facility A and built at two manufacturing sites. It had two RF packages designed and built at Facility C.
- TV-H, designed and assembled at Facility B.

TV-2 Test Vehicle Package I/O /PWB — Fifteen packages from 48 to 784 as listed in Figure 1 were used. The TSOP was used as control for both assembly robustness and environmental reliability comparison. The PWBs were fabricated from FR-4 materials with 6 layers. Microvia design with 3 mil via were consider for all package except the 784 I/O flip chip BGA in one design. In another design, estimated optimized PWB pads with 3 mil microvias were considered. The last PWBs were configured for double-sided assembly. The majority of PWBs had an organic solder preservative surface finish. Hot air solder level (HASL), immersion Au/Ni, and immersion silver were also used.

Solder Paste/Volume — Two types of solder pastes used were no-clean and water soluble (WS). The standard stencil thickness was 6 mil, even though a limited test vehicles were built using stenciles with 5 and 4 mil thicknesses also evaluated. Different stencil aperture design were used. Solder release rate (paste volume measurement) determined for packages with different pitches. Different stencil aperture design were used depending on the pad size.

Package/Test Vehicle Feature — Packages had different pitches, solder ball volumes and compositions, and daisy-chain patterns. All packages were daisy-chained, and they divided into several internal chain patterns. In a few cases,

the daisy chain patterns were irregular and much time and effort was required for the PWB design to match package patterns. The daisy chain pattern on PWB complete the chain loop into the package through solder joints. Several probing pads connected to daisy chain loops were added for failure site diagnostic. The package and PWB daisy chains for a 60 I/O wafer level redistributed CSP and a 208 I/Os FPBGA are shown in Figures 2. The flip chip die was the only device which was underfilled. The test vehicle (TV-2) was 4.5″ by 4.5″ and divided into four independent regions. For single-sided assembly, most packages can be cut for failure analysis without affecting the daisy chains of other packages.

TV-L — This test vehicle had 8 packages from 40 I/Os to 432 I/Os with pitch of 0.8 and 1.27 mm as shown in Figure 3. At the bottom right section of this figure are the RF packages with for SMA connectors (two for each package) which designed and built at Facility C. Detail on RF packages are discussed after thermal cycling data presentation for CSPs. The PWBs had two layers of resin copper coated materials (RCCs) for ease of microvia formation at the top and bottom of a glass epoxy core materials with a total thickness of .065″ (1.62 mm). Microvia technology was used. The test vehicle was 4.5″ by 4.5″.

TV-H — This test vehicle had eight packages from 48 to 280 I/O with pitches of 0.8 mm as shown in Figure 4. The PWB had four layers, thinner than TV-2 and TV-L, with the two RCC layers and an FR-4 Core (1+2+1) with the total thickness of 0.43 mm. Microvia technology was used. Solder paste for assembly was no clean which were applied with a 5 mm thickness stencil. The test vehicle was 4.75″ by 1.85″ with one connector attached for continuous thermal cycling monitoring.

PWB Pad Design for the 60 I/O wafer level CSP and 208/280 I/O FPBGA — In general, non solder mask defined design was used (NSMD) with 2 mil clearance. The PWB pad dimension were varied for the TV-2 and were differ for the 60 I/O control package used in TV-L and TV-H. Design information were as follows:

- TV-L Two sites were allocated for the 60 I/O wafer level package, one location had a pad diameter of 0.3 mm, and the other 0.28 mm as shown in Figure 3 represented by U5 and U6, respectively.
- TV-H Only the U5 location as shown in Figure 4 was used for the 60 I/O wafer level package. The PWB pad diameter was 0.45 mm differ from the estimated optimized version for the TV-L. The 280 I/O FPBGA had two sites, the center and the edge sites, U4 and U2, respectively. The 208 FPBGA had only one site. The PWB pad diameters were 0.3 mm for the 208 and 280 I/O FPBGAs.

Environmental testing — Thermal cycling were performed in the range of –55°C to 125°C with chamber setting and thermal couple reading are shown in Figure 5. The heating and cooling rates were 2° to 5°C/min with a dwell at maximum temperature of more than 10 and a shorter time duration at low temperature. Each cycle lasted 159 minutes.

Monitoring — The test vehicles were monitored continuously during the thermal cycles for electrical interruptions and opens. The criteria for an open solder joint specified in IPC-SM-785, Sect. 7.8, were used as guidelines to interpret electrical interruptions. Generally, once the first interruption was observed, there were many additional interruptions within 10% of the cycle life. In addition, daisy chain opens were verified manually at room temperature after weekly removal of the failed assemblies from chamber.

ENVIRONMENTAL TEST RESULTS

Only limited number of TV-L and TV-H were subjected to this environmental condition. The most current thermal cycle test results to 500 cycles for the TV-L and TV-H are presented here. Cycles-to-failure (CTF) results are compared for a control package assembled on TV-L and TV-H. Also, CTF results of the same I/O and pitch package from two package suppliers are compared. The effect of die on CTF for two packages on the same test vehicle also compared and discussed. Results for other packages and under other conditions are being gathered and will be analyzed and will be presented in the future.

Thermal Cycling Results

Figure 6 shows cycles to first failure for the 60 I/O Wafer level CSP used as control package on two test vehicles. To generate plots, the CTFs were ranked from low to high and failure distribution percentiles were approximated using median plotting position, $F_i = (i-0.3)/(n+0.4)$.
Since all 18 packages failed to 500 cycles for one case, we were able to fit data to a Weibull distribution. Often, two-parameter Weibull distributions have been used to characterize failure distribution and provide modeling for prediction in the areas of interest. The Weibull cumulative failure distribution was used to fit cycles to failure data. The equation is

$$F(N) = 1 - \exp(-(N/No)^m)$$

where

F(N) is the cumulative failure distribution function
N is the number of thermal cycles
No is a scale parameter that commonly is referred to as characteristic life, and is the number of thermal cycles with 63.2% failure occurrence.
The m is the shape parameter and for a large m is approximately inversely proportional to the coefficient of variation (CV) by 1.2/CV; that is, as m increases, spread in cycles to failure decreases

This equation, in double logarithm format, results in a straight line. The slope of the line will define the Weibull shape parameter. The cycles to failure data in log-log were fitted to a straight line and the two Weibull parameters were calculated.

For the wafer level package on TV-H, Weibull parameters for cycles to failure were also generated and plotted in continuous graphs in Figure 6. The Weibull shape parameters, m, was 8 and its characteristic life, No, was 388 cycles. This package failed at higher cycles when assembled on TV-L with much smaller PWB pad design. Except for a low cycles to failure of one assembly at 72 cycles which related to package/assembly defect, the other two failed at 451 and 480 cycles.

For comparison, CTF for two FPBGA packages with 208 and 280 I/Os and a floating pad design package with 280 I/O assembled on TV-H are shown in Figure 7. For the FPBGA package, the relative die size had the most significant affect on CTF. The 208 I/O package with 11.4 mm die size in 15 mm package showed CTF in the range of 176 to 417 cycles with seven out of eight assemblies failed to 500 cycles. The 280 I/O package with 11.8 mm die in 16 mm packages had four failures out of 14 at 303, 336, 339, and 417 cycles. The 208 I/O package with much smaller die size of 9.5 mm showed only two out of ten failures at 476 and 499 cycles.

The 280 I/O package built by another supplier with a new innovative approach to improve reliability showed a similar CTF results to conventional FPBGA package with a large die. This packages built in an R&D environment and required a very elaborate prebake before assembly. Prebake requirements by package supplier due to lack of needed equipment at the assembly facility were not followed. All packages were prebaked at 125°C for 4 hours.

RF Package Characterization Prior to and After Thermal Cycling

High-Speed and RF assemblies tend to be advanced high-value designs that are lagged behind many of the recent innovations in digital packaging technology. Two fundamental issues need to be understood for an application:

- What are the performance characteristics (capacitance, inductance, loss, etc.) of a given interconnect structure?
- Does the proposed interconnect structure change with time?

This part of Consortium investigation aimed to provide some answers to these questions for applications up to 5.0 GHz.

RF Interconnect Structure

Two of the simplest possible RF-Interconnect structures were selected for testing.

- The 50 Ohm RF-Transmission Line consisted of a 50 Ohm circuit trace etched onto Rogers RO4003 laminate material and bonded with Rogers RO4403 adhesive system to form a stripline circuit.
- The 2 GHz RF-Resonator was also a stripline device made with Rogers RO4003. In this case a resonant circuit was etched onto a sheet of laminate followed by bonding with RO4403 adhesive system.

The stripline devices were then processed through drilling, electroless copper plating, copper pattern plating, gold plating, tin/lead plating, etching, and finally the application of solder mask over bare copper. Figure 8 shows a bottom (BGA-side) view of one of the completed 2 GHz RF-Resonator packages. Package pitch is 0.75 mm (30 mil) with 0.2 mm (8mil) balls.

Test Procedures

A network analyzer to characterize the RF interconnect behavior. The equipment is calibrated immediately prior to each test. Known reference signals then transmitted through one of the SMA connectors and changes recorded at the other SMA connector. Reference signals between 50 MHz and 33 GHz were used in this testing. For clarity, only test results in the region between 50 MHz and 5 GHz were reported. During a test run, the analyzer captures needed information with respect to frequency. The data is collected automatically and stored in spreadsheet for data analysis.

Using these data, return loss (S11) and the insertion loss (S21) were calculated using the following relationships:

$$\text{Return Loss} = S_{11} = 20 \log \rho = 20 \log \sqrt{\frac{P_{reflected}}{P_{incident}}}$$

$$\text{Insertion Loss} = S21 = 20 \log \sqrt{\tau} = 20 \log \sqrt{\frac{P_{transmitted}}{P_{incident}}}$$

Plots of Return Loss and Insertion Loss for both the RF-Transmission Line and the 2.0 GHz RF-Resonator are presented in Figures 9.

CONCLUSIONS

These conclusions are based on the limited assembly failure CSPs to 500 thermal cycles in the range of -55°C to 125°C.

- Cycles-to-failure for the same package, assembled on larger pad (0.45 mm diameter).and thinner PWB (0.43 mm) were much lower than those assembled on smaller pad (0.3 mm) and thicker PWB (1.62 mm). This means decrease in thickness has significantly lower effect than decrease in pad size on enhancement of solder joint reliability.
- Cycles-to-failure decreased as die size of FBGA package decreased. The208 I/O FPBGA package with largest relative die size to package dimension (11.4 mm die in 15 mm package) showed lowest cycles to failure, followed by the 280 I/O package with slightly smaller relative die size to package (11.8 in 16 mm).

- A newly package with floating pad design (FPD) showed a similar cycles to failure to the FPBGA package assemblies.
- Return and insertion losses of RF packages with fine pitch ball grid array interconnects for use at 2 to 5 GHz were minimally degraded to 500 thermal cycles.

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2. Achong, A., Rose, D., Ghaffrian, R., et al., "*Impact of Printed Parameters and CSP pitch and I/O on Paste Quality and Volume*", Surface Mount International, Chicago, Sept. 25-28, 2000

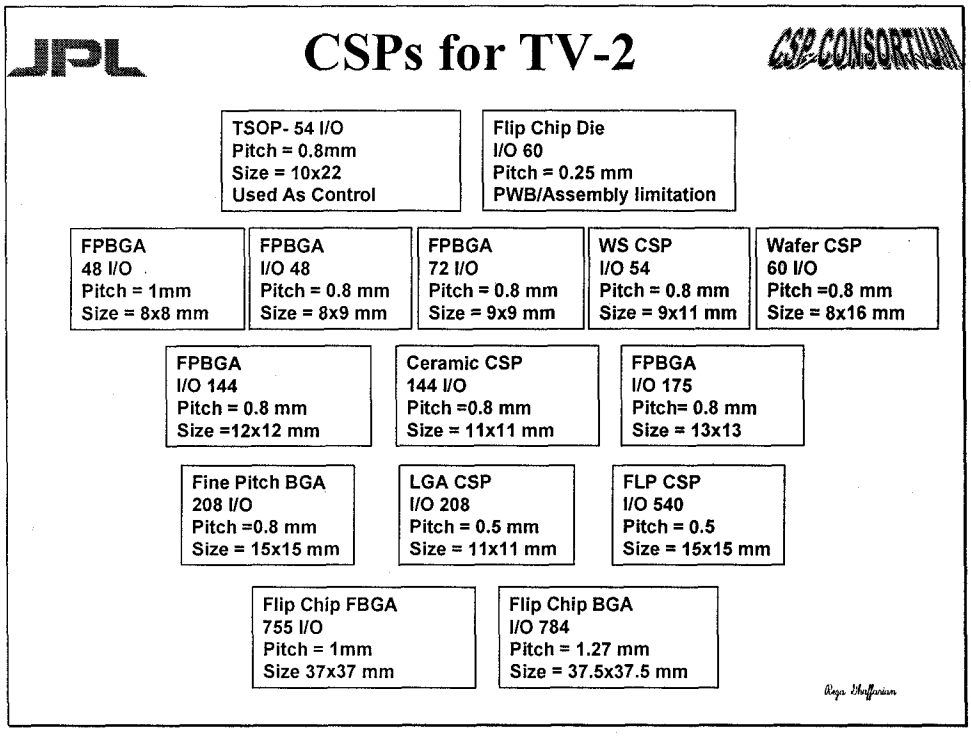
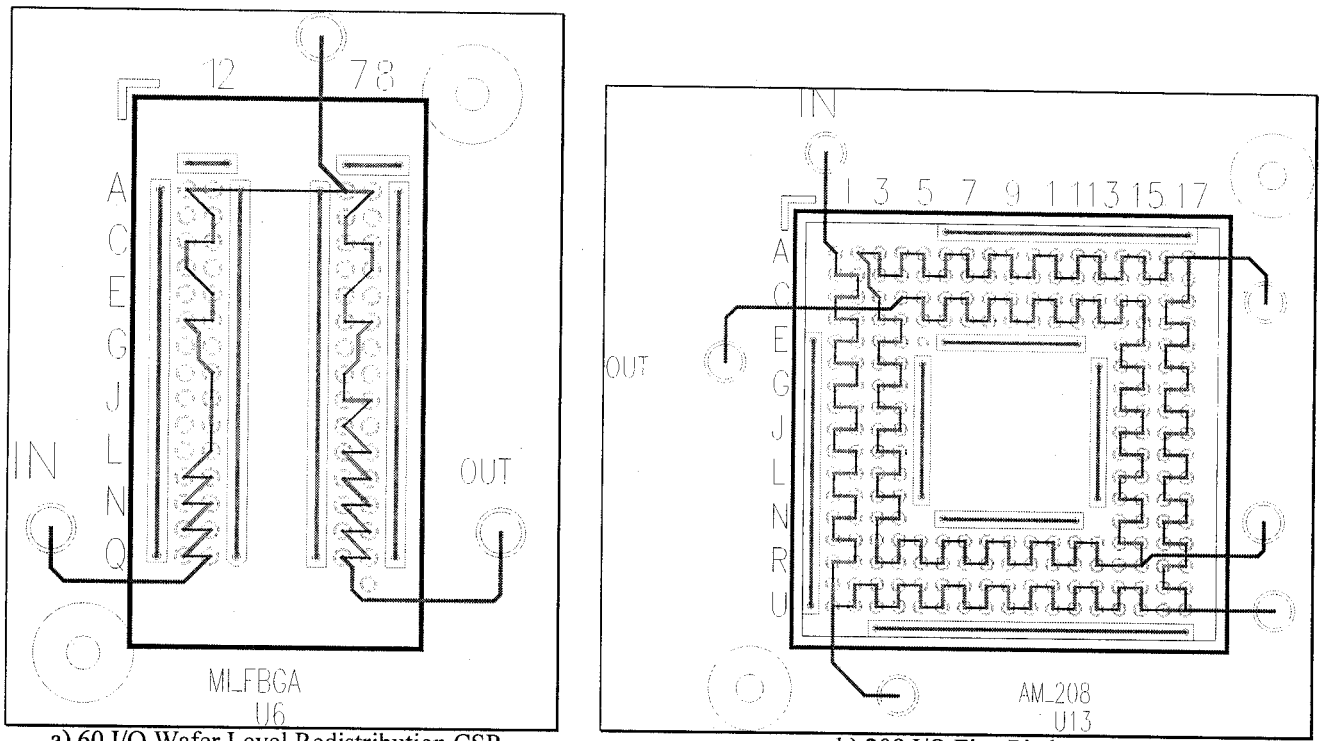


Figure 1 Description of fifteen different CSPs used in TV-2



a) 60 I/O Wafer Level Redistribution CSP

b) 208 I/O Fine Pitch BGA

Figure 2 Package and board daisy chain patterns for two representative packages and probing points for failure diagnostic

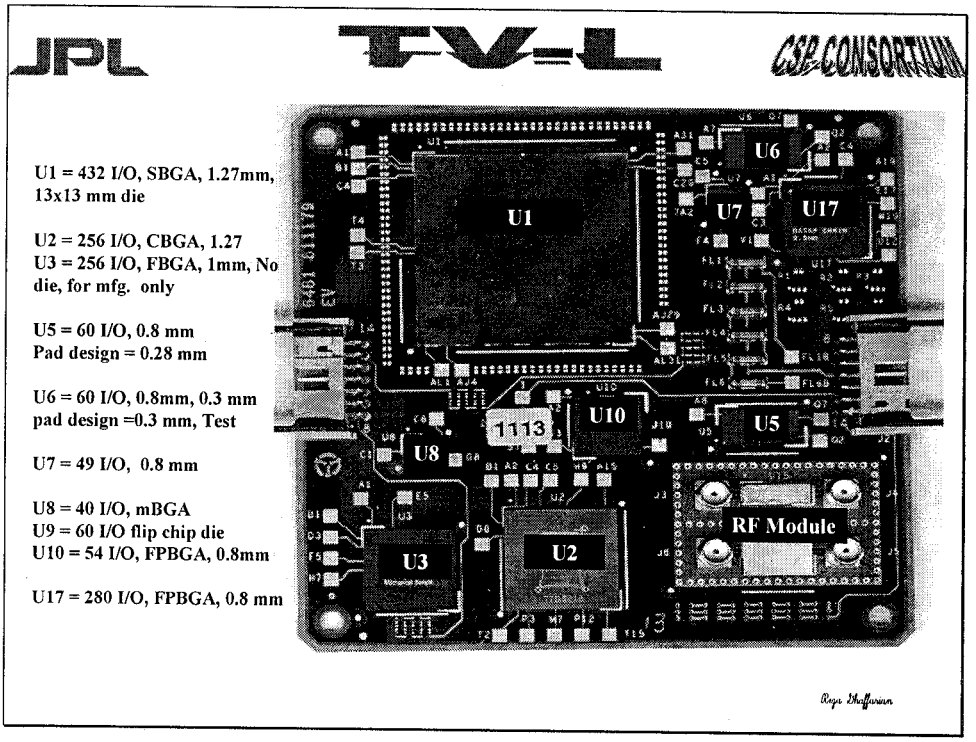
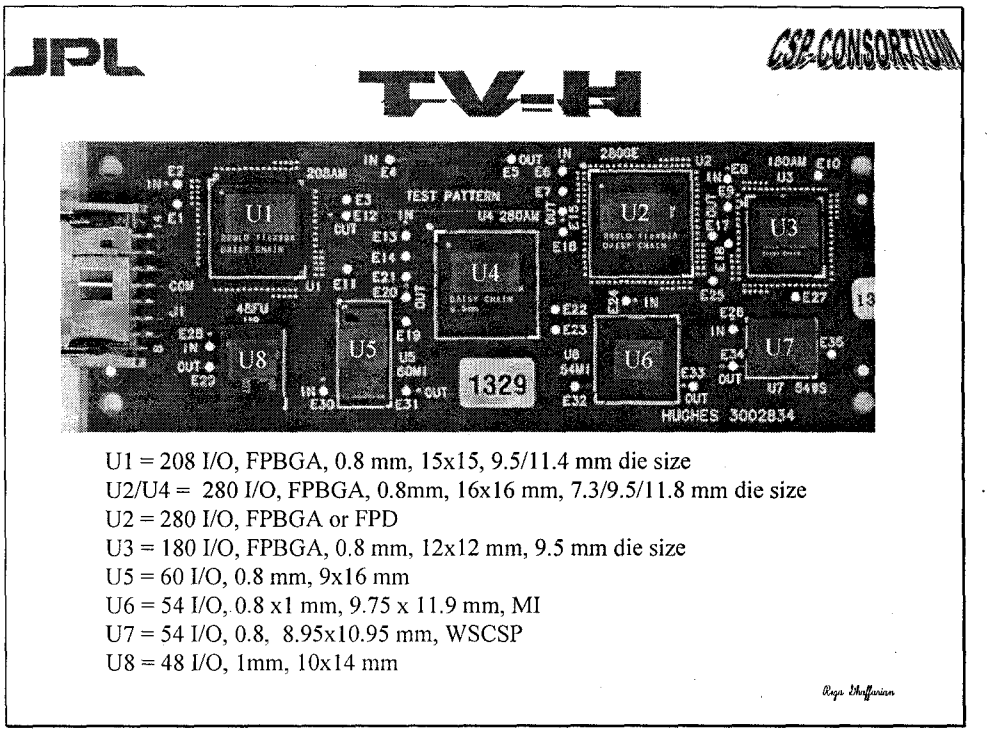


Figure 3 The assembled TV-L with numerous CSP and BGA packages and an RF module



U1 = 208 I/O, FPBGA, 0.8 mm, 15x15, 9.5/11.4 mm die size
U2/U4 = 280 I/O, FPBGA, 0.8mm, 16x16 mm, 7.3/9.5/11.8 mm die size
U2 = 280 I/O, FPBGA or FPD
U3 = 180 I/O, FPBGA, 0.8 mm, 12x12 mm, 9.5 mm die size
U5 = 60 I/O, 0.8 mm, 9x16 mm
U6 = 54 I/O, 0.8 x1 mm, 9.75 x 11.9 mm, MI
U7 = 54 I/O, 0.8, 8.95x10.95 mm, WSCSP
U8 = 48 I/O, 1mm, 10x14 mm

Figure 4 The assembled TV-H with numerous CSP and Fine pitch BGA packages

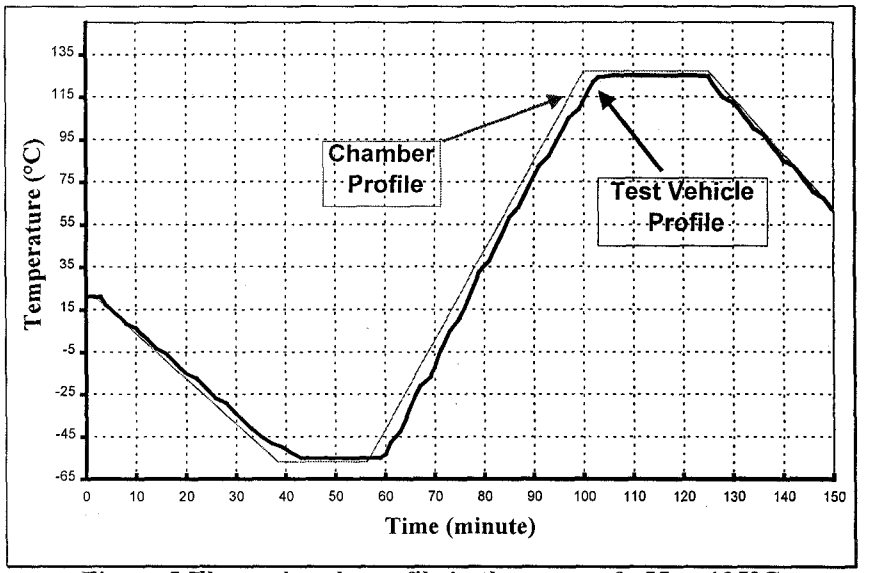


Figure 5 Thermal cycle profile in the range of –55 to 125°C

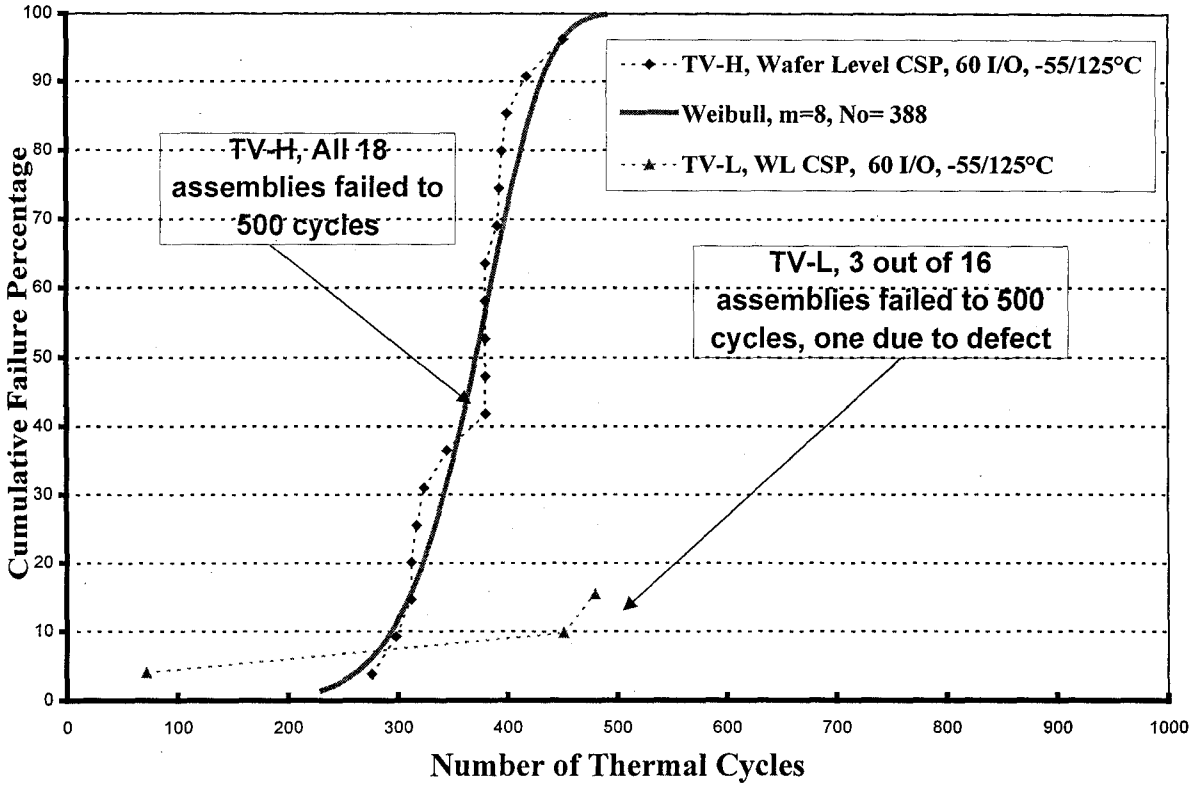


Figure 6 Cumulative failure distribution and Weibull parameter for the control 60 I/O wafer level CSP assembled on TV-H and TV-L and subjected to 500 thermal cycles (-55/125°C)

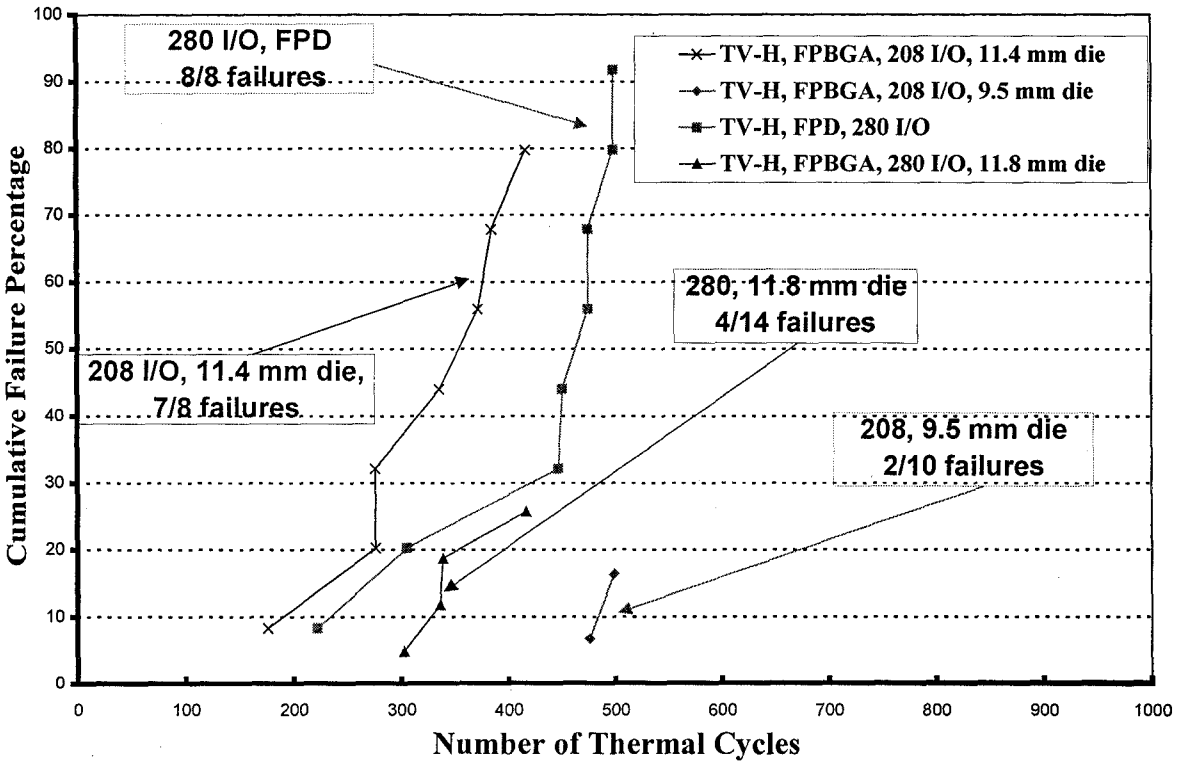


Figure 7 Cumulative failure distributions for several assembled fine pitch BGA package with two package technologies and three die sizes subject to 500 thermal cycles (-55/125°C)

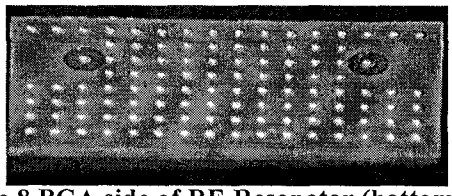


Figure 8 BGA side of RF-Resonator (bottom view)

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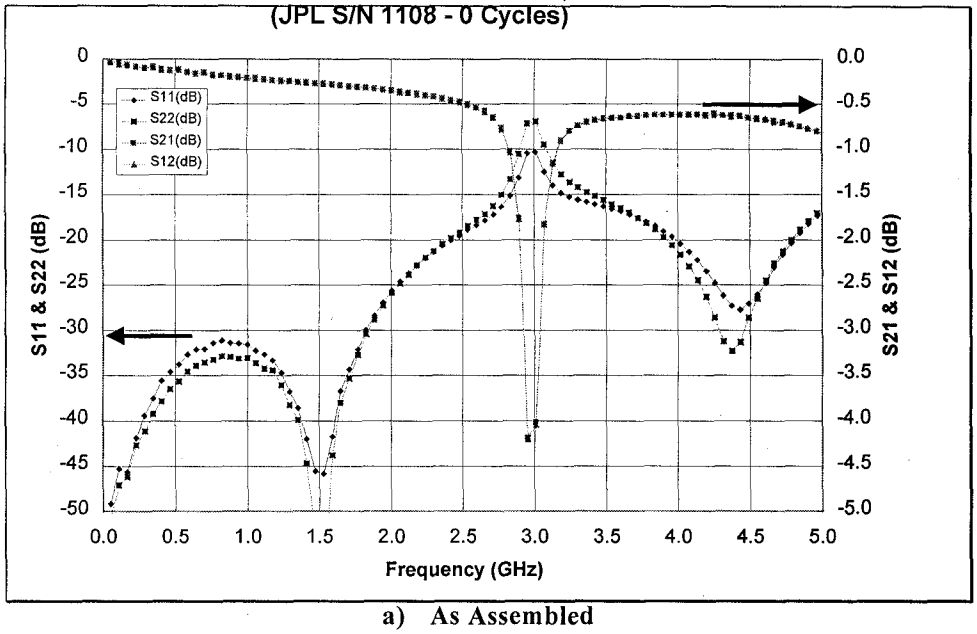
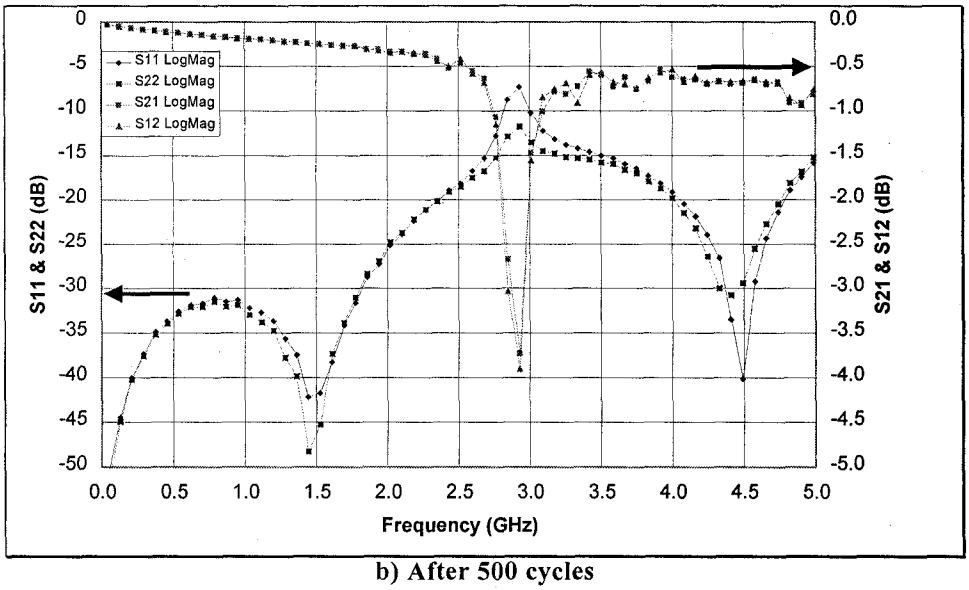


a) As Assembled



b) After 500 cycles

Figure 9 Insertion Loss (S211) and Return Loss (S21) prior to and after 500 Thermal cycles (-55/125°C)